REMARKS

The claims were rejected based on the reference to Rajski under Section 102. However, Rajski was filed after the present application. He does claim priority to a provisional application which is the only priority date preceding the Applicants' filing date. However, a copy of that provisional application is attached and it is clear there is no support for the material cited, namely, paragraphs 66-68. In fact, the corresponding Figures 4B and 4C are not provided in that provisional application.

Therefore, the cited Rajski application is not prior art to the present application and reconsideration is requested.

Respectfully submitted,

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BOX PROVISIONAL PATENT APPLICATION
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WASHINGTON, D.C. 20231

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PROVISIONAL APPLICATION COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 C.F.R. § 1.53(c).

TITLE: FEEDBACK-FREE SEQUENTIAL COMPACTOR OF TEST RESPONSES

Inventor(s)/Applicant(s):

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☒ 13 pages of specification are enclosed.

☒ Provisional Filing Fee Amount:
☒ $160, large entity

☒ A check in the amount of $160.00 to cover the filing fee is enclosed.

☒ The Director is hereby authorized to charge any additional fees which may be required in connection with the filing of this provisional application filed herewith, or credit over-payment, to Account No. 02-4550. A copy of this sheet is enclosed.

☒ Please return the enclosed postcard to confirm that the items listed above have been received.

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FEEDBACK-FREE SEQUENTIAL COMPACTOR OF TEST RESPONSES

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Abstract

This patent proposes a new feedback-free sequential compactor that provides compaction ratios of test responses in excess of 100x even for a very small number of outputs. This is combined with the capability to detect multiple errors, handling of unknown states, and the ability to diagnose failing scan cells directly from compacted responses. The new compactor can be easily configured into a MISR that preserves the same properties. Experimental results demonstrate the efficiency of compaction for several industrial circuits.

1. Introduction

An increasing body of experimental evidence shows that as the semiconductor industry is moving to 0.13 micron technology and beyond, it becomes necessary to use at-speed test and to target transition fault models to achieve acceptable quality of test [1]. The adoption of at-speed testing and the corresponding fault models, combined with the omnipresent exponential increase in gate count, result in accelerated growth of test data volume that is much faster than what is indicated by the Moore's law. In order to address the rapid increase in volume of test data a number of compression schemes have been developed [2], [8], [10], [15].

Detailed analysis of test cube profiles generated by ATPG tools for a wide range of integrated circuits indicates that in many cases, especially where there is no bus contention issues, the average fill rate is well below 1% [10]. With such a very low fill rate it is possible to achieve compression of test stimuli well in excess of 100 times [15]. It is also well known that many designs produce unknown states (often denoted as X states) in test responses, and it is too intrusive to remove them.

All test response compaction schemes, which are currently available, belong to one of two classes.

Infinite input response compaction schemes include polynomial division, counting based techniques, and check sum based methods [18], and all of them are typically used in built-in self-test (BIST) applications. The compaction is usually performed by linear finite state machines such as linear feedback shift registers (LFSRs), multiple input signature registers (MISRs), or cellular automata. These schemes are capable of compacting gigabits of test response data into a small signature, typically 32-, 64-, or 128-bit long, achieving compaction ratios between 10^6 and 10^8. This is possible because an error, once injected into this type of a compactor, will remain there until another group of errors will erase it in the case of aliasing. These schemes require that all values in test responses are known. An unknown state injected into an infinite input response compactor corrupts a signature and renders the test useless. Fault diagnosis is also more complicated and it requires multiple passes with direct access to pre-compacted responses [18].

Space compactors, on the other hand, are combinational circuits, predominantly built of XOR networks, to generate n test outputs from m primary outputs of the circuit under test (CUT), where $n < m$. They offer smaller compaction than the previous class of compactors but they can handle unknown states in responses without circuit modification. The first space only compaction scheme using error codes was proposed in [17]. It was then followed by many other compaction techniques [9], [11], [16], [18]. Some designs, including non-linear spatial compactors, were even customized for a given CUT and for a given test set to eliminate the aliasing phenomenon [3] - [6], [13], [14]. Recently, the X-Compact technique was proposed in [12] to handle simultaneous errors and unknown logic values, both arriving from multiple scan chains.

We introduce here *feedback-free sequential (FFS) compactors* - a completely new class of compaction schemes based on the *finite input response* principle. They have been designed specifically for Embedded Deterministic Test (EDT) technology [15] to handle the following requirements of high quality low cost manufacturing test:

- support of output response compaction with effective ratios in excess of 100 times,
- consistent properties for a whole range of configurations, starting from a single output,
- ability to detect errors of multiplicity 1, 2, 3, and any odd multiplicity with no aliasing,
- very low probability of aliasing (i.e., less than 10^{-6}) of errors of even multiplicity starting from 4 and higher,
- ability to handle unknown states in test responses,
- capability to perform diagnosis, i.e. identify failing scan cells directly from the compacted responses.

The decription is organized as follows. Section 2 de-

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scribes architecture of an FFS compactor. In section 3, error masking is discussed in the absence of unknown states. Section 4 extends the previous analysis to cases where quality of compaction can be compromised by unknown values. In Section 5, diagnostic capabilities of FFS compaction are described. Section 6 introduces an FFS MISR. To conclude, several experimental results are presented in Section 7.

2. FFS compactor

Figure 1 shows an example of an FFS compactor with 16 inputs (observing 16 scan chain outputs), two outputs, and six memory elements – three per output. Although a detailed discussion of properties of FFS compactors will follow in subsequent paragraphs, it is easy to recognize the following characteristics. Every scan cell error can reach memory elements, and then outputs in three possible ways determined by a space-time grid. The spatial part of the grid consists of 2-input XOR gates. Each gate can be labeled as (m, s), where m is the memory element, and s is a scan chain connected through that particular gate to the indicated flip-flop. Thus, for instance, the scan chain no. 7 is connected to the following components of the compactor register: 1, 3, and 6. Moreover, scan chains labeled as 4, 9, 10, 13 15, and 16 also drive the last memory element.

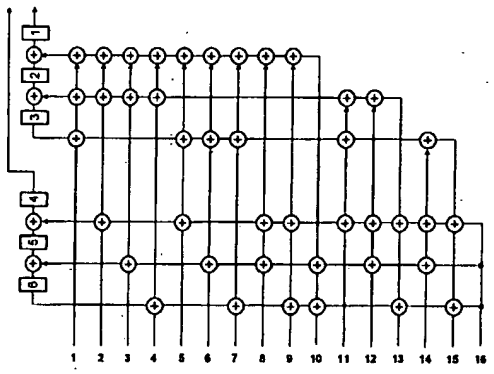

Fig. 1. Example FFS compactor

As can be seen, the compactor does have memory but no feedback. Consequently, any error or unknown state injected into the compactor is shifted out after at most three cycles. Due to fan-outs, every error may propagate to one or two outputs three times. No single X state can mask an error. No odd number of errors or two errors injected at the same time or in different time frames can mask each other completely. Also, single errors injected in each scan propagate to outputs in a different recognizable pattern. It is worth noting, that if one increases the number of memory elements from 6 to, say, 18, the number of scan chains that can be connected to the compactor, and can be still observed on two outputs goes up to 256.

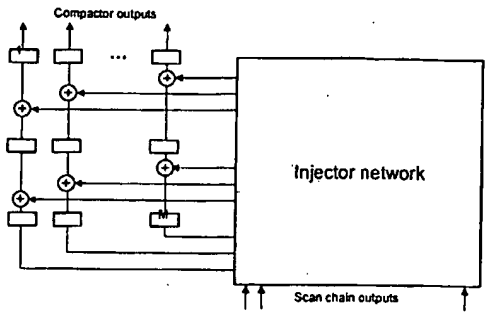

Fig. 2. Architecture of FFS compactor

Architecture. In general (Fig. 2), an FFS compactor can support arbitrary compaction rate for any number of outputs, including architectures with single outputs. The number M of memory elements and injector polynomials indicating how the scan chains are connected to the register flip-flops determine the key properties of an exemplary FFS compactor. In this paper we primarily consider FFS compactors based on polynomials corresponding to certain code words of k-out-of-M codes (for brevity denoted as k/M codes). The 2-output compactor in Fig.1 uses polynomials corresponding to code words of 3/6 code. Here each scan chain is connected through the injector network to three flip-flops in such a way that no other error injected earlier could produce the same error syndrome on the output. For example, the second scan chain in Fig. 1 employs polynomial $P_2 = x^4 + x^2 + x^1$. Note that a shifted version of this polynomial, i.e., $x^5 + x^3 + x^2$, cannot be used because errors injected in two consecutive time frames through such polynomials would cancel each other. On the other hand, polynomial $P_{15} = x^6 + x^4 + x^3$, although a shifted version of P_2, is a valid choice since there is no masking of errors injected through its taps.

Given the number of outputs b, the size of the register M, and the number k of flip-flops driven by each scan chain, the maximum number S of scan chains that can be connected to an FFS compactor is as follows:

$$S = \sum_{i=1}^{b} \binom{M-i}{k-1}$$

For each scan chain there is one or several alternative eligible polynomials. These polynomials correspond to injectors with all taps shifted along the compactor registers with each tap remaining connected to the same output. Only one polynomial from each group can be used. Otherwise 2-error masking may occur. Table 1 provides numerical data obtained from the above formula for 3/M and 5/M polynomials, 1, 2, 4, 8, and 16 outputs and up to 32 memory elements.

A desirable exemplary approach is to use a larger number of memory elements than indicated in the table, and to

select only a subset of valid injector polynomials. In this case, various experimental results indicate that the best performance is achieved by choosing the polynomials randomly rather than following their lexicographic order. With each group of alternative polynomials we select one also at random. Both of the random selections help in balancing the XOR networks. They also provide a better distribution of multiple errors and reduce masking of multiple even errors.

Table 1. The maximum number of observable scan chains in FFS compactors

	Outputs – 3/M polynomials				
M	1	2	4	8	16
3	1	1			
4	3	4	4		
6	10	16	20		
8	21	36	52	56	
10	36	64	100	120	
12	55	100	164	216	
16	105	196	340	504	560
20	171	324	580	920	1136
24	253	484	884	1464	1968
28	351	676	1252	2136	3056
32	465	900	1684	2936	4400
	Outputs – 5/M polynomials				
M	1	2	4	8	16
6	5	6	6		
8	35	50	56	56	
10	126	196	246	252	
12	330	540	736	792	
16	1365	2366	3576	4312	4368
20	3876	6936	11136	14712	15504
24	8855	16170	27000	38136	42448
28	17550	32500	55776	82776	97488
32	31465	58870	103096	158872	197008

Table 2. Maximum number of scan chains in the X-Compact [12] and FFS compactors

Outputs	X-Compact	Conv-16	Conv-32
5	10	395	2035
6	20	440	2360
7	35	476	2660
8	56	504	2936
9	126	525	3189
10	252	540	3420
11	462	550	3630
12	792	556	3820
13	1716	559	3991
14	3432	560	4144

Table 2 shows a significant impact of the sequential part of an FFS compactor on the maximum number of observable scan chains. For example, a compactor with 8 outputs can observe at most 56 scan chains in the X-Compact scheme [12] with the resulting maximum compaction of 7x. An FFS compactor with 3/16 polynomials can observe up to 504 scan chains using 16 flip-flops, and 2936 scan chains connected to 32 flip-flops. The corresponding compaction ratios are 63x and 367x, respectively. This property makes the proposed scheme very well suited for a wide range of modular designs where each block may possess a separate compactor with a very small number of outputs while still providing very high compaction ratios.

3. Error masking in absence of X states

In this section we analyze the masking properties of FFS compactors designed with k/M polynomials. We assume that each polynomial has the same odd number of terms, i.e. 3, 5, 7, etc. The following properties define the capabilities of an exemplary FFS compactor.

Property 1: An FFS compactor with k/M polynomials, for $k = 3, 5, 7, \ldots$ detects errors from one, two or any odd number of scan chains provided that all scan chains produce X-state free responses. The errors can be injected at the same time or at different shift cycles.

Since from each group of alternative polynomials we use only one, there are no shifted versions of injectors, and an effect of an error injected into the compactor cannot be erased by another error injected in the same or later cycle. Two errors can leave an error syndrome in the register that involves 2 bits - if the original errors overlap on 2 positions, 4 bits - if they overlap on one bit, or 6 bits – if they do not overlap. A third error injected from a scan chain can leave the number of affected registers at 1, 3, 5, 7, or 9. A fourth error can set the number of affected registers at 0, 2, 4, 6, 8, 10, and 12. Clearly, 0 indicates 4-error masking. A similar reasoning applies to other odd values of fan-out size k.

As shown above, detection of errors of multiplicity 4 and higher even multiplicity is not guaranteed. To study the size of this problem, extensive experiments were conducted to measure the frequency of 4-error masking and its dependence on the size of registers, the polynomials employed, and the time span of errors. Every measurement was done by conducting Monte Carlo simulations for 100 million error configurations. The following observations are drawn from the experimental results:

- compaction ratio has a marginal impact on the probability of 4-error masking as shown in Table 3 (for the sake of clarity, tables presented in this section contain the number of aliasing cases rather than the probability of its occurrence),
- for the same level of compaction, the number of compactor outputs has a marginal impact on 4-error masking (Table 3),
- polynomials with greater number of terms perform

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better than those with small number of terms; in particular Table 3 shows clear superiority of polynomials 5/M over 3/M ones,

- 4-error masking drops quickly with the increasing number of compactor flip-flops (see Table 4),
- 4-error masking drops quickly with the increasing time span of errors; in all previous experiments errors were injected in the same cycle from scan chain outputs; Table 5 shows experiments where errors are injected over some number of clock cycles defined as an error time span.

Table 3. 4-error masking for 20- and 32-bit registers

C	k	Register size / outputs					
		20/1	20/2	20/4	20/8	32/16	32/32
100x	3	6466	6727	5224	4049	295	274
	5	356	532	529	475	3	6
50x	3	6120	7129	5735	3818	305	278
	5	868	468	540	477	7	3
25x	3	7880	4404	5606	3646	301	273
	5	0	429	491	434	4	7

Table 4. 4-error masking, 100x compaction, 3/M

M	Outputs					
	1	2	4	8	16	32
16	24148	24286	18164	-	-	-
20	6466	6727	5457	4049	-	-
24	3777	2098	2024	1667	1464	-
28	1268	830	890	746	598	-
32	510	549	377	361	295	274
36	295	321	227	117	142	141
40	164	232	97	88	68	78
44	71	76	77	51	54	41
48	57	60	38	32	18	24

Table 5. 4-error masking vs. span, 100x, 3/16, 3/24

Error time span	Register size / outputs				
	16/1	16/2	16/4	24/8	24/16
0	24148	24286	18164	1667	1464
4	5660	1880	410	26	17
8	1692	295	57	7	6
12	561	82	18	5	1
16	213	21	9	0	1
20	76	11	3	0	0
24	44	11	1	0	0
28	32	8	2	0	0
32	21	4	1	0	0

Similar experiments performed with errors of multiplicity 6, 8, 10, 12, 14, and 16 indicate that their masking occurs visibly less often than 4-error masking. These experiments have also been conducted to compare 4-error masking in FFS compactors and combinational compactors with the same number of outputs. For this experiment we selected an X-Compact scheme with 8 outputs and 56 scan chains (i.e., with the maximum number of scans observable in this case as $k = 3$) and three configurations of 8-output FFS compactors. In 100 million cases 4-error masking has occurred 802,146 times in the X-Compact scheme. FFS compactors with 16, 24, and 32 flip-flops have experienced 4-error masking 15696, 1717, and 295 times, respectively. If the number of outputs is increased to 16 (now k is 7), and the number of scan chains is raised to 1600, then the use of the X-Compact lead to 3079 cases of aliasing, while FFS compactors with 24, 32 and 40 memory elements featured the error masking only for the first test setup (21 times). As for the two remaining cases, no aliasing was recorded at all.

A close examination of Table 3 reveals that no 4-error masking was observed for a single output compactor with 20-bit register driven by 25 scan chains. This phenomenon occurs once the number of scan chains becomes small relative to the total number of polynomials that can be deployed for a given compactor. In such a case, there is a good chance that selected randomly polynomials will never allow 4-error masking. However, if one wants to ensure that there is no 4-error masking during one shift independently of the above ratio, then the following design procedure can be applied.

First, generate all suitable polynomials k/M. Their number is given by the formula presented in section 2. Now, suppose a CUT has n scan chains. Hence, choose randomly n polynomials in successive n steps. In each step, the list of polynomials can be regarded as consisting of disjoint three parts: (1) items already approved, (2) polynomials that can be selected during the next step since they do not cause 4-error masking with polynomials chosen earlier, (3) rejected polynomials. Given the list, pick up randomly the next polynomial p from part (2), and then for each pair of selected earlier polynomials (q,r) determine (in a bitwise fashion) the sum $s = p \oplus q \oplus r$. If polynomial s appears on the list (2), move it to part (3), as its usage may lead to 4-error masking. Note, that for single output compactors, which do not use shifted versions of polynomials k/M, this exemplary approach offers particularly efficient performance, since it takes a constant time to locate polynomial s on the list. Indeed, there is a simple mapping between consecutive integers and lexicographically generated k-element sequences chosen from an M-element set, and it can be used here. The approximate maximum numbers of inputs for single-output FFS compactors with M memory elements are given in Table 6. Note that these are the best numbers we obtained by trying several pseudo-random number generators.

4. Error masking in presence of X states

Real circuits, unless designed for BIST application, produce unknown states (X) in their test responses. Because

of limited memory and lack of feedback, FFS compactors are capable handling X states. In fact, states of any FFS compactor and values produced on its outputs depend only on the scan outputs observed in the last few cycles corresponding to a compactor observation window. For a compactor with M bit register and n outputs, the window size or its depth is given by $d = \lceil M/n \rceil$. Thus, any X state injected into the compactor is flashed out in at most d cycles.

Table 6. The maximum number of inputs for single-output FFS compactors with no 4-error masking

M	$k=3$	$k=5$	$k=7$	$k=9$
8	12	12	7	-
9	16	16	11	1
10	18	22	19	9
11	21	28	28	17
12	26	36	36	28
13	29	47	49	43
14	34	58	62	59
15	40	71	82	80
16	44	87	103	104
17	51	106	133	136
18	56	129	169	177
19	60	152	207	226
20	69	183	262	290
21	77	213	323	379
22	81	247	395	465
23	89	281	486	594
24	98	330	586	741
25	105	377	705	930
26	114	435	842	1152
27	123	484	1002	1414
28	132	543	1169	1741
29	139	612	1380	2107
30	150	698	1617	2567
31	161	767	1874	3111
32	176	857	2179	3723

Property 2: In an FFS compactor that uses k/M polynomials, a single error from one scan cell is detected on the compactor outputs in the presence of a single X-state produced by another scan cell.

If there are no X values in responses, an error injected from scan chain output has k alternative ways to be observed on the compactor outputs provided k/M polynomials are employed. Clearly, because of basic properties of these polynomials, a single X state injected into the compactor either at the same scan-out cycle or another one will not be able to mask entirely the error syndrome. However, if multiple X states occur, the error propagation paths can be blocked. As a result, the error may not be observed at all. Assuming that certain number of scan cells produce X states, a quantitative measure of X states ability to mask error syndromes is an observability of scan cells. It is defined as a fraction of scan cells producing errors that can reach the compactor outputs. This quantity depends both on the frequency of occurrence of X states and on the compaction ratio.

Figure 3 shows the impact of X states on observability of scan cells for six FFS compactors with 1, 2, 4, 8, 16, and 32 outputs. All these compactors are comprised of a 32-bit register, they employ 3/32 polynomials, and all of them provide 100x compaction. It is also assumed that the scan length in each case is equal to 100. The percentage of scan cells producing X states varies from 0.01% to 1%. The figure shows four groups of curves:

- the percentage of scan cells not observed (0),
- the percentage of scan cells observed once (1),
- the percentage of scan cells observed twice (2),
- the percentage of scan cells observed three times (3).

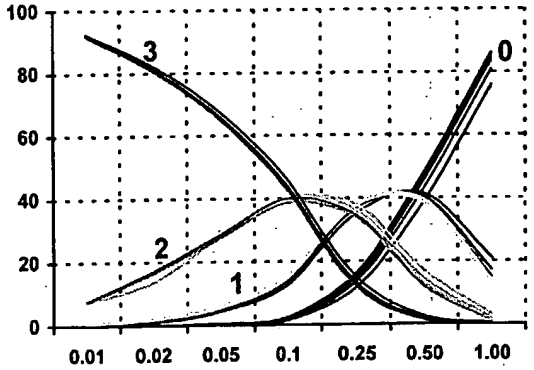


Fig. 3. Observability of scan cell as a function of fraction of cells producing X states

A very strong similarity between curves in each group indicates that the X masking properties do not depend on the number of compactor outputs. There are several distinct regions on this chart. As the number of cells producing X states increases from 0.01% to 0.1%, the number of scan cells that cannot be observed increases from 0.01% to 2%. At the same time, there is reduction of scan cells that are observed 3 times from 92% to 42-45%, and increase of scan cells that are observed twice (up to 40%) and once (around 15%). In the range between 0.1% and 0.25% of cells producing X states, the amount of cells observable twice dominates. In the range between 0.25% and 0.5% most scan cell are observed only once. As the number of scan cells affected by X state keeps increasing, more that 50% of scan cells are not observed anymore.

The compaction ratio determines the number of scan chains observed on each output of the compactor. It also determines how X states impact observability of scan cells. Figure 4 shows the percentage of blocked scan cell for single-output FFS compactor with 32-bit register,

employing 3/32 polynomials, and providing compaction ratios ranging from 10x (the lowest curve) through 25x, 50x, 100x, 250x to 450x (the highest curve). The number of scan cells producing X states varies between 0.01% and 1%. The obtained results indicate that if the compaction ratio increases, then the number of cells affected by X states has to decrease in the same proportion to maintain the scan cell observability at approximately the same level.

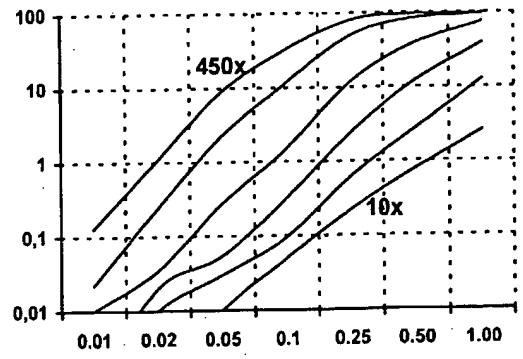


Fig. 4. Blocked scan cells due to X states

Experiments similar to those described in this section were also used to compare observability of scan cells for both the X-Compact scheme and the FFS compactors. Example results are given in Table 7 for compactors with 16 outputs, 1600 scan chains, and $k = 7$. As can be seen, as long as the percentage of scan cells producing X states is smaller than 0.5%, the number of scan cells that can be effectively observed is visibly greater for the FFS compactor (in this example it featured 32-bit register and 7/32 polynomials). Moreover, as shown in the last row of the table, polynomials 3/32 offer superior performance over polynomials with bigger number of terms once the fraction of scan cells with X states becomes larger than 0.1% of their total number.

Table 7. Unobservable scan cells (%) for X-Compact (X) and FFS compaction (C)

	% of scan cell producing X states						
	0.01	0.02	0.05	0.1	0.25	0.50	1.00
X_7	0.061	0.407	1.829	8.093	42.27	84.27	99.41
C_7	0.012	0.036	0.355	2.941	32.10	81.28	99.20
C_3	0.022	0.075	0.501	2.332	15.84	47.56	85.66

5. Diagnostic capabilities

Compactors desirably have the ability to identify the failing scan cells directly from the compacted data to allow simple diagnosis. FFS compactors inherently provide this capability.

Property 3: In an FFS compactor that uses *k/M* polynomials, any single error is uniquely identified on the compactor outputs provided that no X state propagates to the same outputs in any of the observation cycles.

For example, if an error propagates to first input of the compactor in Fig. 1, and no X state propagates to flip-flops 1, 2, and 3, then the error is uniquely identified. This is not always true for multiple errors that interact on the compactor register. For example, an error syndrome observed on output 4, followed by a fault-free cycle and then an error on output 1 may be caused either by double error on inputs 1 and 2, or double error on inputs 7 and 9. In this case, there is ambiguity and the scan chains producing errors cannot be uniquely identified.

To quantify the ability of FFS compactors to diagnose failing scan cells we designed experiments to measure diagnostic resolution for different values of error multiplicity, the size of the register, and polynomials. The resolution is measured by computing the percentage of errors that can be uniquely identified, i.e., errors producing a syndrome that cannot be generated by any other error. Results for errors of multiplicity 4 and FFS compactors of various sizes are presented in Table 8. These results were obtained for the number of scan chains ranging between 16 and 48, two types of polynomials with $k = 3$ and $k = 5$, respectively, and assuming that the time error span is equal to 0.

Table 8. Diagnostic resolution of 4-output FFS compactors for 4-error patterns

M	k	The number of scan chains				
		16	24	32	40	48
12	3	44.01	3.04	0.07	0.00	0.00
	5	52.03	1.18	0.00	0.00	0.00
16	3	100.0	71.54	25.75	7.51	2.06
	5	100.0	79.09	35.18	7.18	0.60
20	3	100.0	95.95	79.97	62.57	39.32
	5	100.0	100.0	95.10	84.78	67.92
24	3	100.0	100.0	99.22	94.75	80.53
	5	100.0	100.0	100.0	98.93	97.51
28	3	100.0	100.0	100.0	98.28	95.48
	5	100.0	100.0	100.0	100.0	99.86
32	3	100.0	100.0	100.0	99.27	98.81
	5	100.0	100.0	100.0	100.0	100.0
36	3	100.0	100.0	100.0	100.0	99.86
	5	100.0	100.0	100.0	100.0	100.0
40	3	100.0	100.0	100.0	100.0	100.0
	5	100.0	100.0	100.0	100.0	100.0

The experiments summarized in Table 8 lead to the following conclusions:

- increasing size of the compactor register improves diagnostic resolution,
- polynomials with higher number of terms (5) perform significantly better than polynomials with smaller

number of terms (3) except for very small compactors and relatively large number of scans,

- diagnostic resolution decreases with the increasing number of scan chains.

The next group of experiments was conducted to determine dependency of the diagnostic resolution on multiplicity of errors. The corresponding results are presented in Fig. 5. It was assumed that FFS compactors have 4 outputs and are driven by 40 scan chains, all employed polynomials have three terms, and the error time span is again equal to 0. As can be seen, the diagnostic resolution is higher for errors of smaller multiplicity. The results also confirm the earlier observation that the increased size of the register may significantly improve the diagnostic resolution.

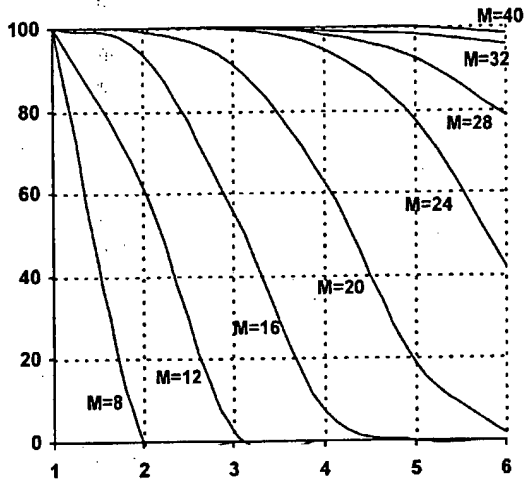


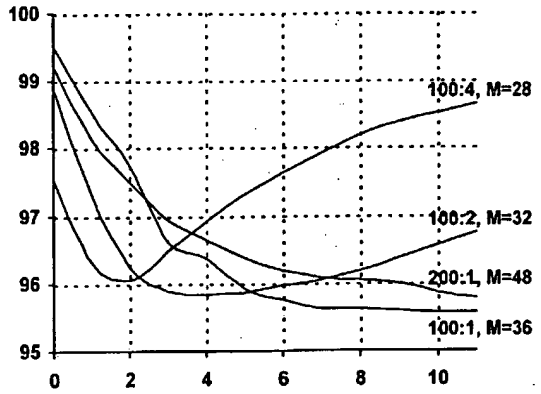
Fig. 5. Diagnostic resolution as a function of error multiplicity for various register sizes

The last group of experiments was aimed at observing a possible impact the compaction ratio may have on the diagnostic resolution. The results presented in Fig. 6 were obtained for 2-error patterns, several FFS compactors with $k = 3$ and the error time span ranging between 0 and 11. Each curve corresponds to a particular compaction ratio indicated by the number of scan chains and the number of outputs. This is accompanied by the size of the register. As can be seen from the figure:

- diagnostic resolution decreases with the increasing compaction ratio; this effect, however can be easily compensated by increasing the size of the register as shown in the figure for compaction 200x,
- diagnostic resolution initially decreases, but then increases with the increasing error time span.

It is worth noting that even in the case of ambiguity, failing scan cells can be determined with a fair precision. For instance, Fig. 6 indicates that for 100x compaction ratio and an error time span of 10, up to 95.57% of error patterns produce unique syndromes using a 36-bit compactor. As for the remaining errors, the same syndrome is shared by two errors in 1.98% of cases. The same syndrome is generated three times by 0.14% of all error patterns. Only 0.009% of errors will have syndromes such that they will be the common ones for four error patterns.

The diagnostic resolution offered by the FFS compactors is clearly superior over that of the X-Compact scheme. Consider an example scheme with 16 outputs and 40 scan chains, each of them driving 16 outputs ($k = 3$). In such a case, a diagnostic resolution achievable with the X-Compact for 4-error patterns is equal to 7.51%. On the other hand, an FFS compactor with a 32-bit register (the number of outputs and the number of scan chains remain



the same) goes up to 100%.

Fig. 6. Diagnostic resolution as a function of time span

6. FFS MISR

Excellent error propagation and diagnostic properties of FFS compactors can make them a good basis to build MISRs. A single output FFS compactor becomes an FFS MISR with the addition of feedback corresponding to a primitive polynomial as shown in Fig. 7 for $h(x) = x^{16} + x^{12} + x^9 + x^6 + 1$. A single gate provides control over two modes of operation of FFS MISR:

- MISR mode where the feedback loop is enabled,
- FFS compaction mode where the feedback is disabled.

In MISR mode the compactor provides the signature computation function well known from a variety of embedded test applications [7], [18]. The injector polynomials 3/16 enhance the performance of the MISR in several ways. Compaction cancellation that occurs when two or even number of errors are injected in the same cycle from scan chains to space compactors, is completely eliminated for 2 errors and drastically reduced for 4 errors and higher even multiplicity. MISR cancellation occurs when even number of errors are injected in different cycles and dif-

ferent scan chains such that the error in the MISR is masked before the feedback connection replicates it into more registers. FFS MISR with 3/16 injector polynomials is immune to MISR cancellation for 1, 2, 3 or any odd number of errors. MISR cancellation is drastically reduced as shown in Tables 3, 4, and 5.

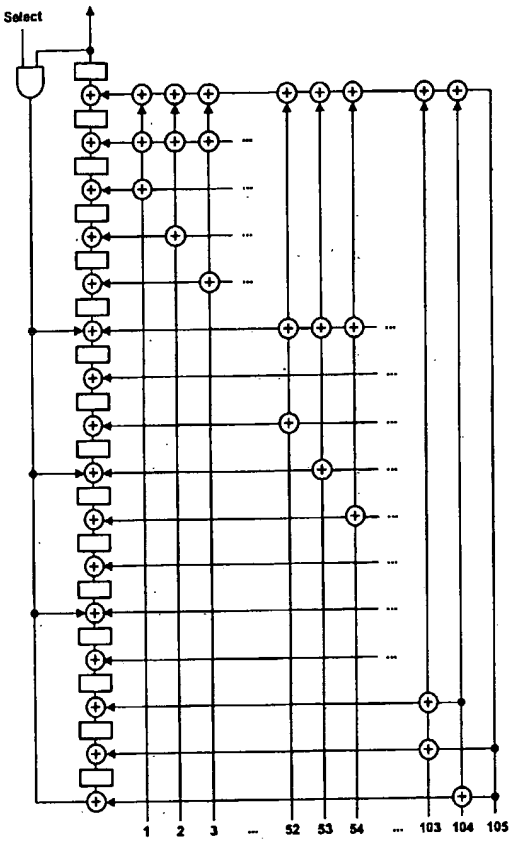


Fig. 7. FFS MISR

The output of the FFS MISR can also be observed in the MISR mode providing diagnostic capabilities not available in conventional MISRs. The diagnosis process using FFS compactor involves a single test session where all patterns are applied and all responses observed on the single MISR output are logged. This error polynomial contains the effects of errors injected from the scan chains and the superposed effects of the feedback polynomial. The effects of the feedback polynomial can be easily removed by multiplying the output error polynomial by the feedback polynomial:

$$E'(t) = E(t+16) + E(t+12) + E(t+9) + E(t+6) + E(t).$$

The FFS compactor mode provides some additional advantages in diagnosis during manufacturing testing. In this case the feedback loop is open and the tester has to log a much smaller number of failing cycles. The errors recorded by the tester correspond directly to $E'(t)$.

7. Experimental results

Performance of the FFS compaction of test responses was further verified on three industrial designs. Their characteristics, including the number of gates and scan cells, as well as the number of scan chains are given in Table 9. The same table is used to summarize the corresponding experimental results. A column indicated by X provides the percentage of unknown states occurring in test responses. These numbers were obtained by simulating complete test sets, and then by evaluating the responses. A commercial ATPG tool generated test sets used in the experiments.

The primary objective of the experimental analysis was to determine observability of scan cells in the presence of unknown states and compare it with the corresponding results obtained for the X-Compact scheme. In all experiments, three different compactors were employed for each design. The first one is based on the X-compact technique. The remaining two devices are FFS compactors labeled C1 and C2, respectively. For each compactor, the number of its outputs as well as the resulting compaction ratio are given in the designated columns of Table 9. The output counts for the X-Compact scheme are determined as shown in [12]. For example, in order to observe 474 scan chains of D2 design, at least 12 outputs have to be used (see also Table 2). Compactors C1 are selected in such a way that they have the same number of outputs as the corresponding X-Compact based circuits. The second group (C2) of FFS compactors offers much higher compaction ratios to show the flexibility of the proposed scheme. The next column lists the number of polynomial terms (k) used to establish the compactors. In the case of the X-Compact scheme, these values were taken from [12], while for all FFS compactors $k = 3$. The M column gives the number of memory elements used to create the sequential part of the FFS compactors (as a purely spatial scheme, the X-Compact does not require any memory elements). For FFS compactors, the number of memory elements is selected so that the total number of usable polynomials is significantly larger than the number of scan chains. It allows reducing the probability of 4-error masking and keeps the diagnosis resolution high. The last two columns show the percentage of scan cells with known values that become unobserved due to the presence of unknown states.

As can be seen, performance of FFS compactors remains consistent with the analysis presented earlier. Indeed, data in Table 9 follow closely those of Fig. 4. For example, when using an FFS compactor C1 in conjunction with design D1, the resulting compaction is about 10x. Given this compaction ratio and 0.79% of scan cells producing

unknown states, a curve in Fig. 4 allows one to anticipate that approximately 4% of scan cells will not be observed. Clearly, the actual data in Table 9 (3.79%) are very close. Furthermore, given the same number of outputs (and thus the same compaction ratio), FFS compactors can guarantee a better observability of scan cells in the presence of unknown states than the X-Compact scheme. In particular, this observation is clearly pronounced for design D2.

Table 9. Experimental results

Design	Gates	DFFs	Scans	X	Compaction scheme	# out	Ratio	k	M	% block		
										Original	Scan masking	Partial
D1	1.6M	45K	96	0.79%	X-Compact	9	10.7	5	0	5.32	-	-
					C1	9	10.7	3	36	3.79	2.29 (1)	0.76 (4)
					C2	4	24	3	36	16.96	4.32 (2)	4.88 (4)
D2	2.5M	57K	474	0.39%	X-Compact	12	39.5	7	0	21.91	-	-
					C1	12	39.5	3	36	4.96	1.06 (5)	0.66 (10)
					C2	4	118.5	3	32	37.28	1.76 (9)	7.08 (10)
D3	2.7M	138K	457	0.09%	X-Compact	11	41.5	5	0	2.07	-	-
					C1	11	41.5	3	33	0.97	0.97 (0)	0.61 (9)
					C2	4	114.3	3	32	8.51	5.12 (6)	3.32 (10)

It appears that many industrial designs feature unknown states largely clustered, i.e., a vast majority of unknown values are produced by a small fraction of scan chains. As shown in Table 10, the cumulative percentage of unknown states expressed as a function of the number of scan chains they come from levels off very quickly. In all examined designs, 10 scan chains were sufficient to capture the significant majority of unknown values.

Table 10. Distribution of unknown values

	1	2	3	4	5	10
D1	43.7	78.5	83.4	85.0	86.6	93.9
D2	21.9	36.3	48.8	59.6	70.0	95.5
D3	10.9	18.9	25.4	31.7	37.7	60.6

Following the above observation, one can enhance performance of the FFS compaction by gating those scan chains that are prone to capturing unknown values. Since the number of scan chains that yield the majority of unknown states is small, this approach, while preventing the unknown states from being injected into the compactor, does not compromise a test quality. The enhanced FFS compactor is illustrated in Fig 10. In addition to the actual compactor, it is comprised of R registers, where R is a small integer determined by the number of scan chains. In the reported experiments, R = 5 if there are no more than 100 scan chains in the design. Otherwise, one extra register is added for every additional 100 scan chains. The distribution network is used to mask the scan chains whose addresses are stored in the registers. There is a bit associated with each register indicating whether the corresponding address is valid for the current pattern. Clearly, for each pattern, up to R addresses are scanned in to mask the respective scan chains. As a result, a small fraction of unknown values are shifted into the compactor, and hence the overall scan cells observability is improved.

The observability of scan cells assuming masking of scan chains is given in the last column of Table 9 (data in the brackets indicate the average number of scan chains that were masked for each pattern). As can be seen, ability to control certain scan chains improves visibly the resulting observability. In particular, compactors C2 perform much better than before. For example, the original C2 of D1 has 16.96% unobserved known responses, while this rate reduces to 4.32% if up to 5 scan chains are masked for each pattern. This result is even better than that of the X-compaction scheme for D1 while the compaction ratio of the X-compaction is much lower. For D2 and D3, the enhanced FFS compactors achieve over 100x compaction with good observability. It is worth noting that even for D2 whose responses have a few unknown values, the scan chain masking can reduce the number of unobserved scan cells to a very low level.

In the embedded test environment, the address registers have to be loaded by the on-chip decompressor. As an example, consider compactor C2 of D3. Since this design has 457 scan chains, 9 bits are needed to address each chain. There is also a flag associated with each register, and therefore test data required for each pattern amount to $10 \times 6 = 60$ bits. As for design D3, the average number of specified bits for each pattern is 360, and thus the resulting compaction ratio is approximately $138K / 360 \approx 383x$. Taking into account data required to control the compaction process, the actual compression ratio drops to the acceptable level of $138K / (360 + 60) \approx 327x$. The same analysis can be conducted for designs D1 and D2. The average number of specified bits per pattern for D1 and D2 are 1500 and 940, respectively, and hence the compaction ratio for D1 remains virtually the same, while the compaction ratio for D2 changes from 60 to 55.

Another modification of the scheme is shown in Fig. 8. Here a switching network is capable of observing all scan

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chains in a group of selected ones when the flag "All observed" is enabled. If the flag is disabled then one scan chain is selected by the scan address register and this scan chain is either blocked or it is the only scan observed from this group depending on the "Block" flag.

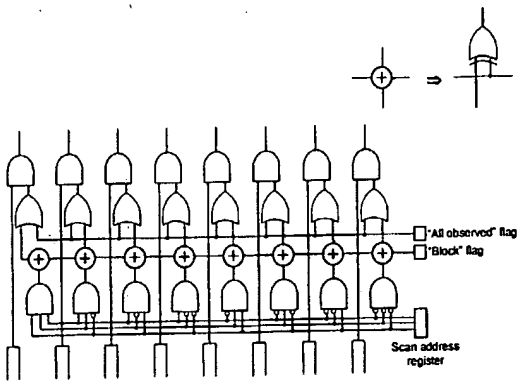

Fig. 8. Switching network with complete blocking of selected scan chains

It has been observed that in some cases it is beneficial to only block the fanout branches partially rather than completely. This way there are fewer X states injected into the compactor but at the same time the partially blocked scan chains maintain some observability of their scan cells that have known values. Table 9 shows that in cases where the percentage of scan cells originally not observed is relatively low, like for C1 compactors in design D1 and D2, and both C1 and C2 compactors in design D3, the partial blocking scheme gives lower percentage of blocked scan cells than the compactor with complete blocking of selected scan chains. The scheme that performs the partial scan blocking function is shown in Fig. 9.

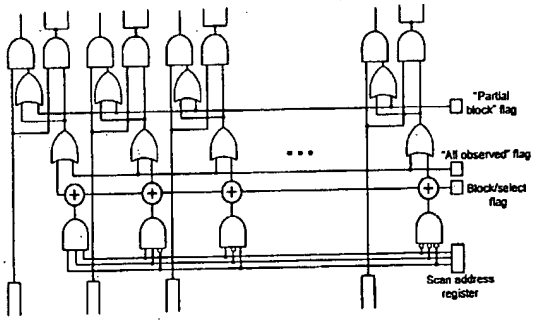

Fig. 9. Switching network with partial blocking of selected scan chains

To guarantee that all known values are observed when needed, a bypass mode can be added to an FFS compactor as shown in Fig. 10. In the bypass mode, the outputs are used to directly observe n scan chains, where n is the number of outputs. The same address registers that are employed to mask scan chains in the compaction mode, select the scan chains that are observed in this mode. The distribution network translates the addresses and wires the designated chains to the outputs.

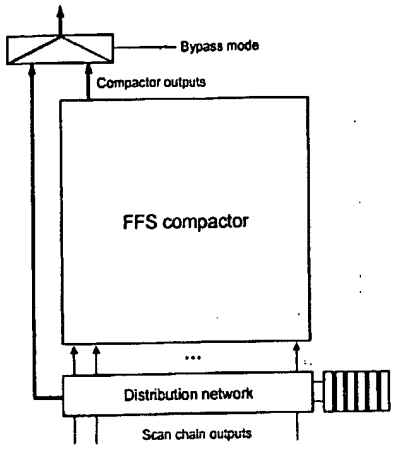

Fig. 10. Enhanced architecture of compactor

In a more universal solution, the bypass mode is determined on an individual basis as shown in Fig. 11 for one output. Here once the Bypass flag allows the bypass mode, the "All observed" flag has to disabled. Then the scan address register selects the scan chain for bypass. The selected register is also blocked from the FFS compactor to minimize any negative impact of X states and simplify diagnostics.

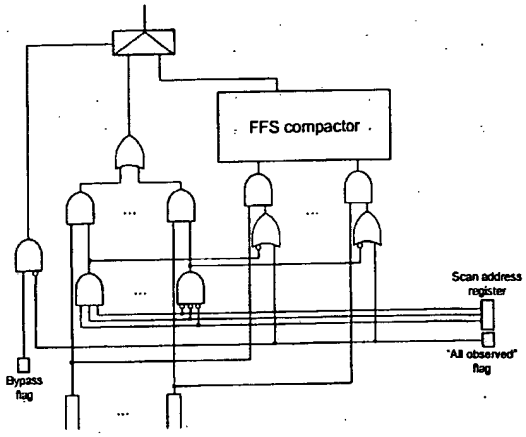

Fig. 11. Individually controlled bypass

There are two distinct ways to program the compactor: (a) without taking into account any information where the faults propagate to, and (b) with information taken from the ATPG tool that generates the patterns. The examples discussed so far represent the first case. The main information that was considered included location of X states. A completely new level of benefits can be realized if the compactor is programmed by the ATPG tool that creates

the patterns and keeps track of the scan cells where the faults propagate to. In this case the focus of setting the controls is on making sure that the faults do not get blocked while propagating through a compactor. This ATPG driven approach is applicable to all the schemes discussed earlier. Another exemplary scheme that can benefit from ATPG driven approach is shown in Fig. 12. Here the switching network allows different configurations of connections of scan chains to the compactor inputs. Even though each configuration may block some percentage of scan cells some configurations might be much better in observing scan cells that ATPG identifies as the ones carrying fault information.

Table 11. Unobservable scan cells (%)

	D1	D2	D3
0	44.20	49.70	23.74
1	41.82	21.17	10.81
2	29.62	10.24	6.06
3	29.01	4.16	3.50
4	28.80	1.85	2.26
5	28.49	1.13	1.54
6	25.79	0.61	1.11
7	25.73	0.30	0.86
8	25.65	0.19	0.63
9	13.48	0.11	0.41
10	13.39	0.08	0.29
11	12.29	0.06	0.24
12	12.25	0.04	0.19
13	10.13	0.04	0.13
14	8.93	0.04	0.11
15	8.91	0.03	0.09

It turns out that if we have multiple configurations available they are very few scan cells that will remain unobservable for all of them. Table 11 shows that for design D3 with 457 scan chains observed on 2 outputs (compaction ratio – 228x) on average there are 23.74% of scan cells not observed for one configuration, but only 0.09% scan cells that are not observed in all 16 configurations. It means that for any one of the 99.91% scan cells it is possible to find one configuration that observes it. A scheme implementing this method is shown in Fig. 12.

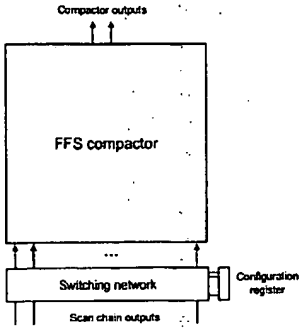

Fig. 12. Switching network with multiple configurations of scan assignments to compactor inputs

A modification of this scheme is shown in Fig. 13. Here the configuration is modified as the scan shifting is taking place. Initially the counter can be loaded as in the previous scheme.

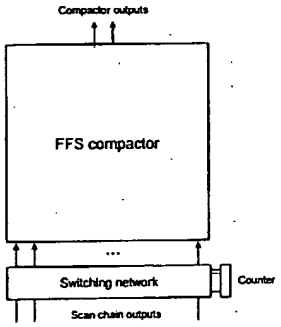

Fig. 13. Scheme of Fig. 12 with configurations selected by means of counter

In some applications internal scan chains can shift at much higher frequency than the tester controlling the test. In such cases it is advantageous to operate the compactor at the speed of the tester and use one of two schemes shown in Fig. 14 and 15 to match the bandwidths. In the scheme in Fig. 14 scan chains are shifted at higher frequency and the data unloaded from scan chains is first shifted to the serial input parallel output (SIPO) register. Only after the SIPO registers are loaded the compactor samples the data. This way the total number of scan chains routed on the chip can also be reduced at the expense of the registers. The scheme in Fig. 15 operates on the same principle except the data is directly taken from multiple scan cells including those that are not on the output.

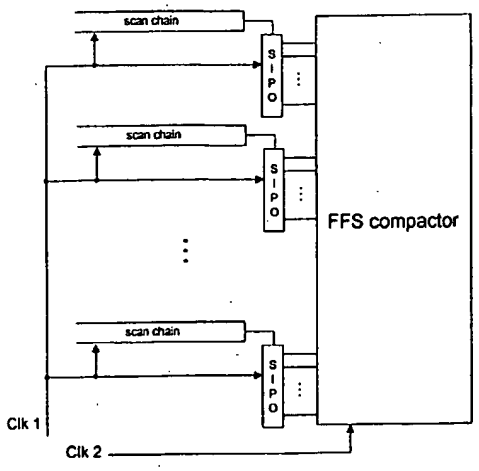

Fig. 14. FFS compactor driven by scan chains through serial input parallel output registers

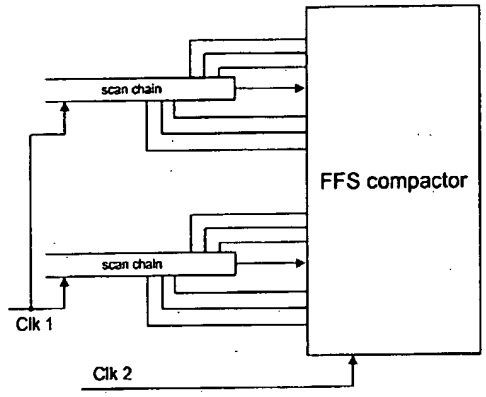

Fig. 15. FFS compactor driven by several scan cells of the same scan chains

8. Conclusions

In this paper we introduced examples of a new compaction scheme that has several new properties matching extremely well the requirements of embedded deterministic test. The illustrated exemplary FFS compactors can provide very high compaction ratios in excess of 100x. The modular design of the exemplary embodiments is very well suited for the SoC design style where each core or a block can have a separate compactor with a very small number of outputs, small number of global signals, and simplified routing. The illustrated schemes support very high quality of test by providing very good observability of scan cells in the presence of unknown values and detection of multiple errors. These exemplary schemes also provide the ability to identify failing scan cells directly from the compacted responses of the faulty circuit. This feature, when included in an embodiment, simplifies the tester requirements and the whole manufacturing test flow. Examples of a new architecture of a MISR built on an FFS compactor were also presented. One property of a desirable example of the FFS MISR is its ability to identify failing scan cells by observing only one output. Experimental results conducted on three exemplary industrial designs demonstrate that as long as the percentage of scan cells that produce X states is less than 0.25% this compaction scheme can provide compression in excess of 100x without any intrusion to the design.

The invention is directed toward novel and unobvious features and aspects of the embodiments of the new compactor and methods described herein. The disclosed features and aspects of the embodiments can be used alone or in various novel and unobvious combinations and subcombinations with one another.

References

1. G. Aldrich and B. Cory, "Improving test quality and reducing escapes," *Fabless Forum Magazine*, March 2003.
2. C. Barnhart, V. Brunkhorst, F. Distler, O. Farnsworth, A. Ferko, B. Keller, D. Scott, B. Koenemann, and T. Onodera, "Extending OPMISR beyond 10x scan test efficiency," *IEEE Design and Test*, vol. 19, No. 5, pp. 65-73, 2002.
3. B. Bhattacharya, A. Dmitriev, M. Gossel, and K. Chakrabarty, "Synthesis of single-output space compactors for scan-based sequential circuits," *IEEE Trans. CAD of IC*, vol. 21, No. 10, pp. 1171-1179, 2002.
4. K. Chakrabarty, B. T. Murray, and J. P. Hayes, "Optimal space compaction of test responses," *Proc. ITC*, pp. 834-843, 1995.
5. K. Chakrabarty and J.P. Hayes, "Test response compaction using multiplexed parity trees", *IEEE Trans. CAD of IC*, vol. 15, No. 11, pp. 1399-1408, 1996.
6. K. Chakrabarty, "Zero-aliasing space compaction using linear compactors with bounded overhead," *IEEE Trans. CAD of IC.*, vol. 17, No. 5, pp. 452-457, 1998.
7. G. Hetherington, T. Fryars, N. Tamarapalli, M. Kassab, A. Hassan, J. Rajski, "Logic BIST for large industrial designs: real issues and case studies," *Proc. ITC*, pp. 358-367, 1999.
8. F. Hsu, K. Butler, and J. Patel, "A case study on the implementation of the Illinois scan architecture," *Proc. ITC*, pp. 538-547, 2001.
9. W-B. Jone and S.R. Das, "Space compression method for built-in self-testing of VLSI circuits," *Int. Journal of Computer Aided VLSI Design*, vol. 3, pp. 309-322, 1991.
10. B. Koenemann, C. Barnhart, B. Keller, T. Snethen, O. Farnsworth, and, D. Wheater, "A SmartBIST variant with guaranteed encoding," *Proc. ATS*, pp. 325-330, 2001.
11. Y.K. Li and J.P. Robinson, "Space compression methods with output data modification," *IEEE Trans. CAD of IC*, vol. 6, No. 2, pp. 290-294, 1987.

EXPRESS MAIL LABEL NO. EV 295230744 US
DATE OF DEPOSIT: February 13, 2003

12. S. Mitra and K. S. Kim, "X-compact: an efficient response compaction technique for test cost reduction," *Proc. ITC*, pp. 311-320, 2002.

13. I. Pomerantz, S. Kundu, S. M. Reddy, "On output response compression in the presence of unknown output values," *Proc. DAC*, pp. 255-258, 2002.

14. B. Pouya and N.A. Touba, "Synthesis of zero-aliasing elementary-tree space compactors" *Proc. VTS*, pp. 70-77, 1998.

15. J. Rajski, J. Tyszer, M. Kassab, N. Mukherjee, R. Thompson, H. Tsai, A. Hertwig, N. Tamarapalli, G. Mrugalski, G. Eide, J. Qian, "Embedded deterministic test for low cost manufacturing test", *Proc. ITC*, pp. 301-310, 2002.

16. S.M. Reddy, K. K. Saluja, and M. G. Karpovsky, "A data compression technique for built-in self-test," *IEEE Trans. Comput.*, vol. 37, No. 9, pp. 1151-1156, 1988.

17. K. K. Saluja and M. Karpovsky, "Testing computer hardware through data compression in space and time," *Proc. ITC*, pp. 83-88, 1983.

18. P. Wohl, J. A. Waicukauski, T. W. Wiliams, "Design of compactors for signature-analyzers in built-in self-test," *Proc. ITC*, pp. 54-63, 2001.